ABSTRACT OF THE DISCLOSURE

A deep trench self-alignment process for an active area of a partial vertical cell. A semiconductor substrate with two deep trenches is provided. A deep trench capacitor is formed in each deep trench, and an isolating layer is formed thereon. Each trench is filled with a mask layer. A photoresist layer is formed on the semiconductor substrate between the deep trenches, and the photoresist layer partially covers the mask layer. The semiconductor substrate is etched lower than the isolating layer using the photoresist layer and the mask layer as masks. The photoresist layer and the mask layer are removed, such that the pillar semiconductor substrate between the deep trenches functions as an active area.